ABSTRACT

DATA PROCESSING APPARATUS AND METHOD

A data processing apparatus maps input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The data processor includes an interleaver memory which reads-in the predetermined number of data symbols for mapping onto the OFDM carrier signals. The interleaver memory reads-out the data symbols on to the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on to the carrier signals. The set of addresses are generated from an address generator which comprises a linear feedback shift register and a permutation circuit. In order to provide a 4k mode for an OFDM modulated system such as a Digital Video Broadcasting (DVB) standard such as DVB-Terrestrial (DVB-T) or DVB-Handheld (DVB-H) standards, a generator polynomial for the linear feedback shift register of $R_i'[10] = R_{i-1}'[0] \oplus R_{i-1}'[2]$ is provided with a permutation order which has been established by simulation analysis to optimise communication performance via typical radio channels.

[Fig. 7]